**APPLICATION NOTE** 

# **Configuring the PAC52XX Multi-Mode Power Manager**

**Power Application Controller®** 

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# **1** OVERVIEW

The PAC52XX family of Power Application Controller<sup>®</sup> (PAC) is highly optimized for controlling and powering next-generation smart energy appliances, devices and equipment. The PAC family of controllers integrates management of many system functions for these applications, including power management.

Each device in the PAC52XX family of controllers contains a Multi-Mode Power Manager<sup>™</sup> (MMPM). The MMPM provides "all-in-one" efficient power management solutions for multiple types of power sources. The MMPM integrates control for a switching power supply that can support buck, SEPIC or AC/DC Flyback modes up operation, as well as up to four linear regulated voltage supplies. In addition, the switching power supply can also be disabled, if the application can power the IC directly.

The table below shows the PAC52XX family of devices, which voltage ranges are supported as well as which converter topologies are supported.

Device	Input Voltage (DC/DC disabled)	DC/DC	Input Voltage (DC/DC enabled)	Buck	Boost	SEPIC	AC/DC Flyback
PAC5210	4.5V – 16V	Х	5.2V – 52V	Х	Х		Х
PAC5220	4.5V – 16V	Х	5.2V – 52V	Х	Х		Х
PAC5222	4.5V – 16V	Х	5.2V – 44V	Х		Х	Х
PAC5223	4.5V – 18V	Х	5.2V – 72V	Х		Х	Х
PAC5225	4.5V – 18V	Х	5.2V – 72V	Х		Х	Х
PAC5250	4.5V – 16V	Х	5.2V – 52V	Х	Х		Х
PAC5253	4.5V – 16V	Х	5.2V – 52V	Х	Х		Х
PAC5255	4.5V – 16V	Х	5.2V – 52V	Х	Х		Х

This document shows examples of how to configure the firmware in the PAC52XX device to support the DC/DC mode, as well as some application examples for each of the supported power topologies shown above.



## 2 **FIRMWARE CONFIGURATION**

The MMPM allows the user to configure the operational mode of the DC/DC converter via firmware on the MCU in the PAC52XX. The MMPM allows the user to select if the DC/DC controller is enabled or disabled. The administrative state of the DC/DC controller is selected by the **SOC.PWRCFG.SMPSOFF** bit.<sup>1</sup>

#### 2.1 Disabling the DC/DC Controller

To disable the DC/DC controller, the MCU should set the **SOC.SCFG2.SMPSOFF** bit to a 1. With this configuration, the application must supply the PAC52XX on the VP pin.

The following code will set this bit, without changing any of the other fields:

#### 2.2 Enabling the DC/DC Controller

To enable the DC/DC controller, the MCU should set the **SOC.SCFG2.SMPSOFF** bit to a 0. When the DC/DC controller is enabled, the VP output voltage is generated according to the setting of the **SOC. SCFG2.VP** field.

For example, in the PAC5223 the user may set the following VP output voltages:

- 5V (00b)
- 9V (01b)
- 12V (10b)
- 15V (11b)

The following code will clear the **SOC.SCFG2.SMPSOFF** bit and set a VP output voltage of 15V without changing any of the other fields:

```
reg_value = pac5xxx_file_register_read(0x15); /* Read SOC.PWRCFG */
reg_value &= ~0x20; /* Set SMPSOFF bit to 0 */
reg_value |= 0xC0; /* Set VP to 3 (15V) */
pac5xxx tile register write(0x15, reg value); /* Write SOC.PWRCFG */
```

Each of the supported DC/DC topologies will need to customize the firmware configuration of the MMPM. See the sections below for more detail on each of these topologies.

<sup>&</sup>lt;sup>1</sup> The default value for the DC/DC controller is 0 (enabled)



# 3 BUCK MODE

#### 3.1 Block Diagram

The block diagram below shows how a DC/DC buck topology may be implemented with the PAC52XX.



### 3.2 MMPM Configuration

The Input Voltage is supplied on VHM and output is generated on VP.

The MMPM allows you to configure several parameters for the operation of the DC-DC:

- VP output voltage
- VHM clamp voltage
- Switching frequency
- Maximum duty cycle

The VP output voltage and Switching Frequency are dependent on the application, and inductor for the power supply. For a buck mode DC-DC, the maximum duty cycle isn't very important so any value may be used.

To configure the MMPM for a buck mode DC-DC, the following configuration is recommended:

- Set SOC.PWRSTATCFG.PWRUNLOCK to 1b to enable write access to SOC.SCFG and SOC.SCFG2
- Set **SOC.SCFG.VHMCLAMPSEL** to 0b to set the VHM voltage clamp to 20V
- Select the switching frequency by writing the **SOC.SCFG.FMODE** and **SOC.SCFG.FSWM** fields to the appropriate values (see below)
- Enable the DC-DC by setting the **SOC.SCFG2.SMPSOFF** bit to a 0b
- Select the output voltage of the DC-DC (VP) by writing the **SOC.SCFG2.VP** value to the appropriate value (see below)

The DC/DC switching frequency may be selected by the values shown in the table below.



#### Configuring the PAC52XX MMPM **Power Application Controller®**

FMODE	FSWM	Switching
		Frequency
0	0	45kHz
	1	50kHz
	2	55kHz
	3	62.5kHz
	4	72.25kHz
	5	82.5kHz
	6	100kHz
	7	125kHz
1	0	181kHz
	1	200kHz
	2	220kHz
	3	250kHz
	4	289kHz
	5	330kHz
	6	400kHz
	7	500kHz

The VP output voltage may be selected from the SOC.SCFG2.VP field as shown below.

VP	VP voltage setting
00b	5V
01b	9V
10b	12V
11b	15V

#### 3.3 Application Example

A typical configuration for a DC-DC in buck mode would be:

- Switching Frequency: 500kHz ٠
- MAXDUTY: Min off time: 500ns •
- VHM Voltage clamp disabled •
- VP output voltage: 12V ٠

In order to configure the MMPM for the above configuration, the following code fragment may be used:

pac5xxx\_tile\_register\_write(ADDR\_PWRCTL, 0x40); pac5xxx\_tile\_register\_write(ADDR\_PSTATSET, 0x80); pac5xxx\_tile\_register\_write(ADDR\_SCFG, 0x3E); pac5xxx\_tile\_register\_write(ADDR\_PWRCFG, 0x8E);

- // Set MCUALIVE (indicate alive to in case of reset)
  // Set PWRUNLOCK bit to allow firmware to modify SCFG & PWRCFG
  // Set VCLAMPSEL=20V, Fs=500kHz, DMIN=500ns
  // Set DC/DC enabled, VP=12V, VCC18, TON, TRESET, VSYSILIM



# 4 SEPIC MODE

#### 4.1 Block Diagram

The block diagram below shows how a DC/DC SEPIC topology may be implemented with the PAC52XX.



### 4.2 MMPM Configuration

The Input Voltage is supplied on VHM and output is generated on VP.

The MMPM allows you to configure several parameters for the operation of the DC-DC:

- VP output voltage
- VHM clamp voltage
- Switching frequency
- Maximum duty cycle

The VP output voltage and Switching Frequency are dependent on the application, and inductor for the power supply. For a SEPIC mode DC-DC, the maximum duty cycle must be set to a maximum of 75% or a minimum off time of 500ns.

To configure the MMPM for a SEPIC mode DC-DC, the following configuration is recommended:

- Set SOC.PSTATSET.PWRUNLOCK to 1b to enable write access to SOC.SCFG and SOC.SCFG2
- Set **SOC.SCFG.VCLAMPSEL** to 0b to set the VHM voltage clamp to the lower voltage setting
- Select the switching frequency by writing the **SOC.SCFG.FMODE** and **SOC.SCFG.FSWM** fields to the appropriate values (see below)
- Select a 500ns minimum duty cycle off time by writing **SOC.SCFG.FMODE** to 0b and **SOC.SCFG.DMAX** to 0b
- Enable the DC-DC by setting the **SOC.SCFG.SMPSOFF** bit to a 0b
- Select the output voltage of the DC-DC (VP) by writing the SOC.SCFG2.VP value to the appropriate value (see below)



The DC/DC switching frequency may be selected by the values shown in the table below.

FMODE	FSWM	Switching Frequency
Ob	000b	45kHz
	001b	50kHz
	010b	55kHz
	011b	62.5kHz
	100b	72.25kHz
	101b	82.5kHz
	110b	100kHz
	111b	125kHz
	000b	181kHz
	001b	200kHz
	010b	220kHz
1b	011b	250kHz
	100b	289kHz
	101b	330kHz
	110b	400kHz
	111b	500kHz

The VP output voltage may be selected from the SOC.SCFG2.VP field as shown below.

VP	VP voltage setting	
00b	5V	
01b	9V	
10b	12V	
11b	15V	

#### **Application Example** 4.3

A typical configuration for a DC-DC in SEPIC mode would be:

- Switching Frequency: 125kHz •
- MAXDUTY: Min off time: 500ns •
- VHM Voltage clamp disabled
- VP output voltage: 15V •

In order to configure the MMPM for the above configuration, the following code fragment may be used:

pac5xxx\_tile\_register\_write(ADDR\_PWRCTL, 0x40); pac5xxx\_tile\_register\_write(ADDR\_PSTATSET, 0x80); pac5xxx\_tile\_register\_write(ADDR\_SCFG, 0x2E); pac5xxx\_tile\_register\_write(ADDR\_PWRCFG, 0xCE);

- // Set MCUALIVE (indicate alive to in case of reset)
  // Set PWRUNLOCK bit to allow firmware to modify SCFG & PWRCFG
  // Set VCLAMPSEL=20V, Fs=125kHz, DMIN=500ns
- // Set DC/DC enabled, VP=15V, VCC18, TON, TRESET, VSYSILIM



# 5 AC/DC FLYBACK MODE

#### 5.1 Block Diagram

The block diagram below shows how a AC/DC Flyback topology may be implemented with the PAC52XX.



#### 5.2 MMPM Configuration

The Rectified Input Voltage is supplied on VHM and output is generated on VP.

The MMPM allows you to configure several parameters for the operation of the AC/DC Flyback converter:

- VP output voltage
- VHM clamp voltage
- Switching frequency
- Maximum duty cycle

The VP output voltage and Switching Frequency are dependent on the application, and inductor for the power supply. The VHM clamp should be set to 20V.

To configure the MMPM for a buck mode DC-DC, the following configuration is recommended:

- Set SOC.PWRSTATCFG.PWRUNLOCK to 1b to enable write access to SOC.SCFG and SOC.SCFG2
- Set SOC.SCFG.VHMCLAMPSEL to 0b to set the VHM voltage clamp to 20V
- Select the switching frequency by writing the **SOC.SCFG.FMODE** and **SOC.SCFG.FSWM** fields to the appropriate values (see below)
- Enable the DC-DC by setting the SOC.SCFG2.SMPSOFF bit to a 0b
- Select the output voltage of the DC-DC (VP) by writing the SOC.SCFG2.VP value to the appropriate value (see below)



The DC/DC switching frequency may be selected by the values shown in the table below.

FMODE	FSWM	Switching
	<u>^</u>	Frequency
0	0	45kHz
	1	50kHz
	2	55kHz
	3	62.5kHz
	4	72.25kHz
	5	82.5kHz
	6	100kHz
	7	125kHz
1	0	181kHz
	1	200kHz
	2	220kHz
	3	250kHz
	4	289kHz
	5	330kHz
	6	400kHz
	7	500kHz

The VP output voltage may be selected from the SOC.SCFG2.VP field as shown below. Note that for high-voltage Buck operation, only 12V and 15V will be valid selections.

VP	VP voltage setting	
00b	n/a	
01b	n/a	
10b	12V	
11b	15V	

#### 5.3 Application Example

A typical configuration for a DC-DC in SEPIC mode would be:

- Switching Frequency: 181kHz ٠
- MAXDUTY: Min off time: 500ns •
- VHM Voltage clamp enabled (20V) •
- VP output voltage: 15V •

In order to configure the MMPM for the above configuration, the following code fragment may be used:

pac5xxx\_tile\_register\_write(ADDR\_PWRCTL, 0x40); pac5xxx\_tile\_register\_write(ADDR\_PSTATSET, 0x80); pac5xxx\_tile\_register\_write(ADDR\_SCFG, 0x10); pac5xxx\_tile\_register\_write(ADDR\_PWRCFG, 0xC0);

- // Set MCUALIVE (indicate alive to in case of reset) // Set PWRUNLOCK bit to allow firmwre to modify SCFG & PWRCFG // Set VCLAMPSEL=20V, Fs=181kHz, DMIN=500ns // Set DC/DC enabled, VP=15V



# 6 RECOVERING PAC52XX WHEN DC/DC DISABLED

Certain problems may prevent the DC/DC from starting properly, resulting in an unresponsive PAC device. For example, if the user firmware disables the DC/DC controller, but the PCB is designed to only operate in SEPIC mode, the PAC device will not be powered, and it cannot be recovered until it is powered.

The PCB will attempt to start up the DC/DC when it is powered up. But if the PAC52XX has disabled the internal DC/DC controller, then the power supply on VP will never come up, causing the PAC to not power up so that the firmware can be changed.

In order to work around this issue, VP must be supplied directly. The steps below show how to do just this.

#### 6.1 Remove the Inductor

Remove the inductor in the DC/DC. In the schematic below (for a SEPIC converter), this is component L1.



This will separate the switching supply from VHM.



#### 6.2 Short VHM to VP

In order to power the PAC52XX directly from VP, the PCB must have the VHM and VP pins shorted.

#### 6.3 Supply VP

Supply the PAC52XX on VP with 12V-15V. This will allow the PAC52XX device to start.

At this point, the user may erase the firmware, so that the DC/DC is not disabled. Then the VHM to VP short and inductor may be disabled.



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